(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 671 767 A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 95107360.0

(51) Int. Cl.6: H01L 23/525

(22) Date of filing: 10.07.90

This application was filed on 16 - 05 - 1995 as a divisional application to the application mentioned under INID code 60.

(30) Priority: 24.08.89 US 398141

(43) Date of publication of application:
13.09.95 Bulletin 95/37

(60) Publication number of the earlier application in accordance with Art.76 EPC: 0 414 361

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IT LI LU NL SE

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(54) Semiconductor antifuse structure and method.

(57) A method for forming an array of antifuse structures on a semiconductor substrate which previously has had CMOS devices fabricated thereupon up to first metallization. A fuse structure is formed as a sandwich by successively depositing a bottom layer of TiW, a layer of amorphous silicon, and a top layer of TiW. The amorphous silicon is formed in an antifuse via formed in a dielectric layer covering the bottom layer of TiW. First metallization is deposited and patterned over the top layer of TiW. An intermetal dielectric layer is formed over the fuse array and second metal conductors are formed thereupon. An alternative embodiment includes forming an oxide sidewall spacer around the periphery of an antifuse structure. Connection resistance to the bottom layer of TiW is lowered by using a number of vias between the second-metal conductors and the bottom layer of TiW in a row of an array of antifuse devices.

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FIGURES 2A and 2B are plan views of portions of an array of antifuses.

FIGURES 3A through 3D are cross-sectional views showing various stages in the formation of an antifuse according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to those embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. The structures described are formed using well known semiconductor fabrication techniques.

FIGURE 1 shows an antifuse structure 70 formed on a silicon semiconductor substrate 72 that has been processed through standard CMOS process steps up through contact formation. The antifuse structure 70 is fabricated as a sandwich structure. A first layer of TiW 76 is formed on the substrate. A layer 78 of preferably amorphous silicon or polysilicon is formed on the first layer of TiW 76. A second layer of TiW 80 is formed over the silicon layer 78. A silicon dioxide sidewall spacer 82 is formed to surround the periphery of the sandwich structure. A first metal, or conductive layer, 84 is formed over the top surface of the second layer of TiW 80 and the sidewall spacer 82. A standard intermetal dielectric layer 86 is formed over the first metal layer 84. A second metal aluminum layer 88 is formed and patterned over the standard dielectric layer 86. The second metal connects the first TiW layer through vias at regular intervals on a fuse array. The second TiW is removed between adjacent first metal lines as the first metal is patterned, thus forming self-aligned vertical fuse structures.

FIGURES 2A and 2B (in more detail) show partial plan views of some of the elements of a portion of an array of antifuse devices,

as shown in cross-section in FIGURE 1. A number of first-metal aluminum conductors (typically shown as 102a-102j) are formed as parallel strips with a certain pitch, or spacing, therebetween. Beneath the first metal conductors are formed antifuse structures (typically indicated as 104) each of which has a second layer of TiW beneath the first metal conductors. When the first metal aluminum layer is masked and etched, the TiW in the areas 106 between the antifuses 104 is also removed to leave only amorphous silicon areas 106 between the antifuses 104. This provides a row of self-aligned antifuses, spaced apart by the first metal pitch, as shown in the FIGURES. Additional rows of antifuses are located parallel to that row of antifuses. A second-metal aluminum conductor 108, crosses over and is perpendicular to the first metal conductors 102. A via 110 (typically shown) extends from the second metal conductors (typically shown as 108a-108f) to respective first layer of TiW at the bottom of the antifuse structure. The vias provide a plurality of connections between the second-metal conductor and the first TiW for a row of antifuse structures. This provides a reduced-resistance connection for the antifuse structures. Consequently, TiW is usable for the bottom conductor of the antifuses while still having lower connection resistances.

FIGURE 2A shows the vias 110 spaced apart every 5 antifuses, or 6 metal-one pitches. In the prior art, external connections, using metal-two conductors to the bottom TiW layer would be made only at an end of a bottom conductor line. Using TiW in that connection arrangement would result in higher resistance connections. Using a number of connection vias for second-metal connections, as indicated in the drawing significantly reduces the connection resistance to any one of the antifuse structures.

FIGURES 3A-3D show various process stages in the formation of an antifuse structure elements forming an array of antifuses similar to those shown in FIGURE 1.

FIGURE 3A shows a standard CMOS-processed wafer, processed up to first metallization. Over the surface of the substrate is then formed a protective layer 116 preferably 500-1000 Angstroms of TiW, or aluminum, to protect various previously formed circuit components and active devices formed on the substrate. A masking and etching step removes that portion of the protective layer 116 in the fuse area 118 in which a fuse structure is to be formed.

FIGURE 3B shows a first layer 120 of 2500 A of TiW deposited in the fuse area 118. A layer 122 of 1000-2000 A of amorphous or polysilicon is deposited over the TiW layer 120. A second layer 124 of 1000-2000 A of TiW is deposited on the layer 122. A masking and etching step is then used to etch the TiW layers 120,124 and the silicon layer 122 to form a vertical antifuse sandwich 126 as indicated in the drawing.

FIGURE 3C shows the fuse structure 126 with an oxide sidewall spacer 128 surrounding the periphery of the fuse structure. The sidewall spacer 128 is formed by a plasma oxide deposition over the fuse structure. A subsequent isotropic etching of the oxide layer produces the sidewall 128 as

a second layer (124) of TiW formed on said layer of antifuse silicon, said first and second layers of TiW and said layer of antifuse silicon forming a vertical antifuse sandwich structure;

a sidewall spacer (128) formed adjacent to and surrounding the periphery of said antifuse sandwich structure;

a first metal layer (138) overlying said sidewall spacer and said antifuse sandwich structures;

an intermetal dielectric layer formed over said first metal layer; and

a second metal connected to the first TiW layer through a via formed in said intermetal dielectric layer to provide reduced connection resistance to said first TiW layer.

7. The antifuse structure as claimed in claim 6 wherein said layer of antifuse silicon includes a layer of amorphous silicon.

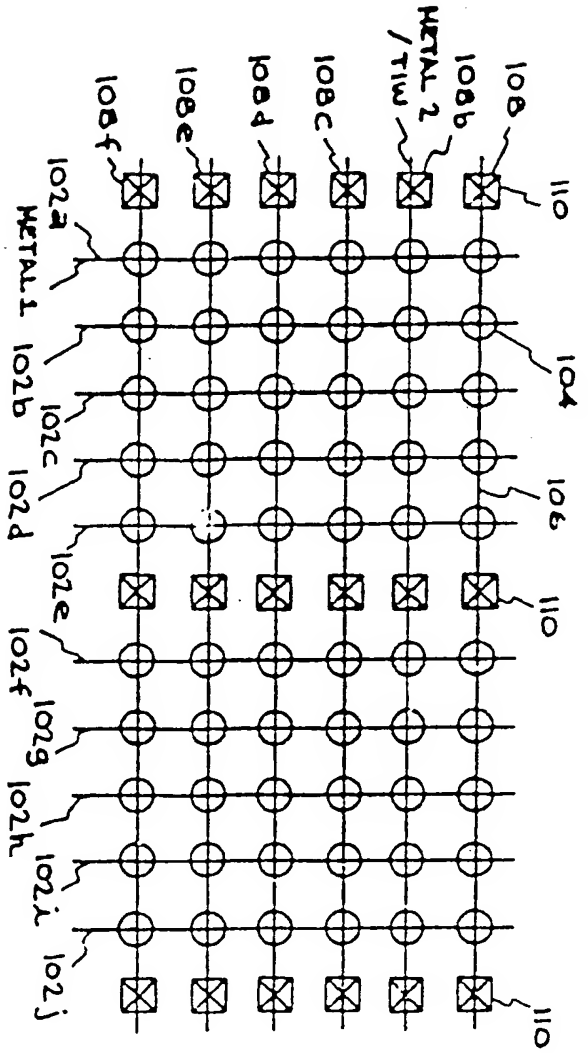
108f
108e
108d
108c
METAL 2 / TiW
108b
108
110
102a METAL 1
102b
102c
102d
102e
102f
102g
102h
102i
102j
104
106
110
110

FIG. 2A